



MX23L12810A

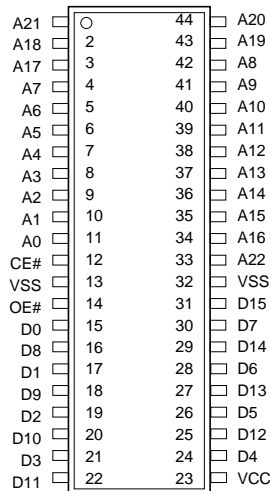
128M-BIT PAGE MODE MASK ROM (SOP)

FEATURES

- Bit organization
 - 8M x 16 (word mode)
- Fast access time
 - Random access:100ns (max.)
 - Page access:25ns (max.)
- Page size
 - 8 words per page
- Current
 - Operating:25mA
 - Standby:15uA
- Supply voltage
 - 2.7V ~ 3.6V
- Package
 - 44 pin SOP (500mil), Pb-free, RoHS
- Temperature
 - 0°C ~ 70°C
- Process
 - 0.18um

PIN CONFIGURATION

44 SOP



PIN DESCRIPTION

Symbol	Pin Function
A0~A22	Address Inputs
D0~D15	Data Outputs
CE#	Chip Enable Input
OE#	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

ORDER INFORMATION

Part No.	Speed	Package	Grade	Remark
MX23L12810AMC-10G	100ns	44 pin SOP	Commercial	Pb-free
MX23L12810AMC-12G	120ns	44 pin SOP	Commercial	Pb-free



MODE SELECTION

CE#	OE#	D0~D15	Mode	Power
H	X	High Z	-	Stand-by
L	H	High Z	-	Active
L	L	D0~D15	Word	Active

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 2.7V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	0.7xVCC	VCC+0.3	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC	-	25mA	f=5MHz, CE#=VIL, OE#=VIH all output open
Standby Current (CMOS)	ISTB	-	15uA	CE#>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 2.7V~3.6V)

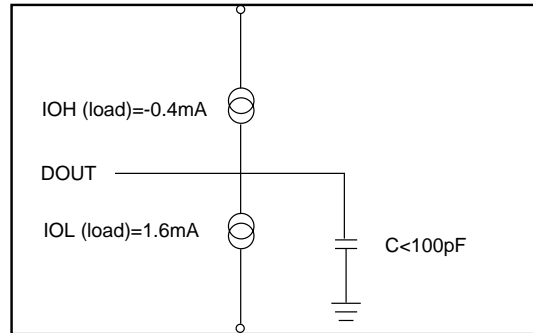
Item	Symbol	23L12810A-10		23L12810A-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tCE	-	100ns	-	120ns
Page Access Time	tPA	-	25ns	-	25ns
Output Enable Time	tOE	-	25ns	-	25ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note:

- Output high-impedance delay (tHZ) is measured from OE# or CE# going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.
- Operating current is measured under Non-Return to Zero (NRZ) test pattern.

AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	5ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure



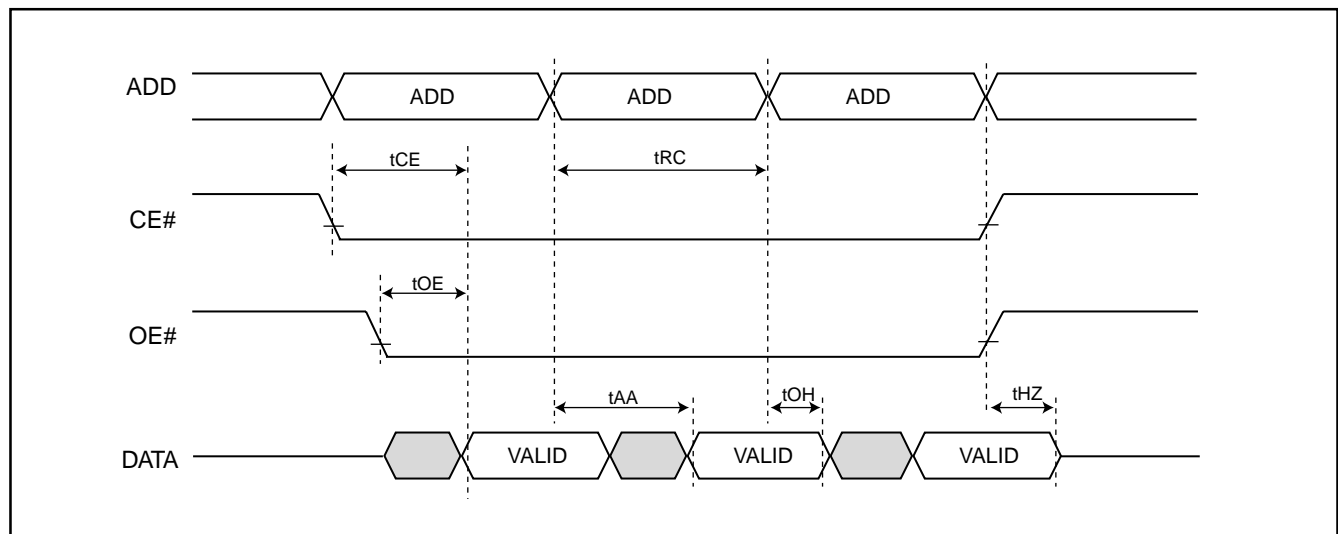
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

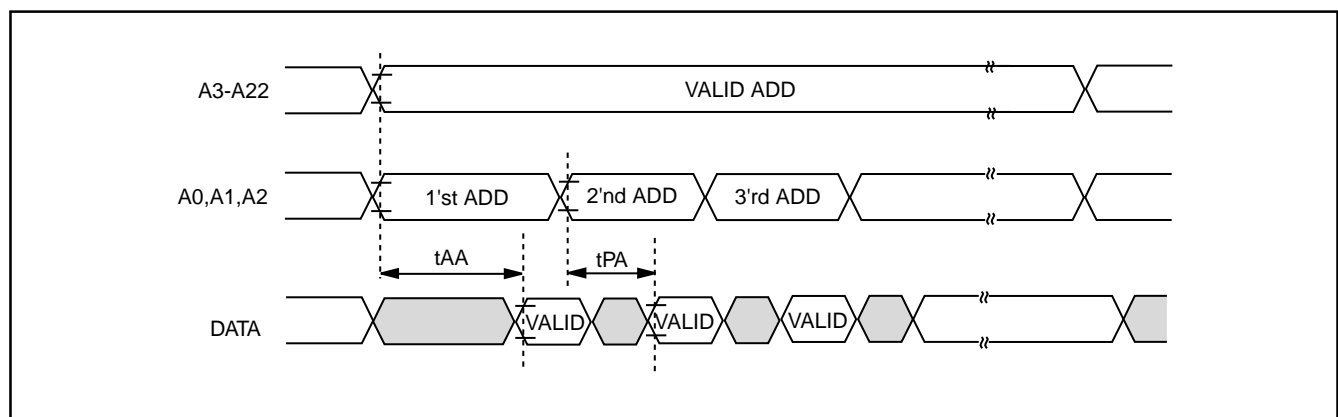
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ

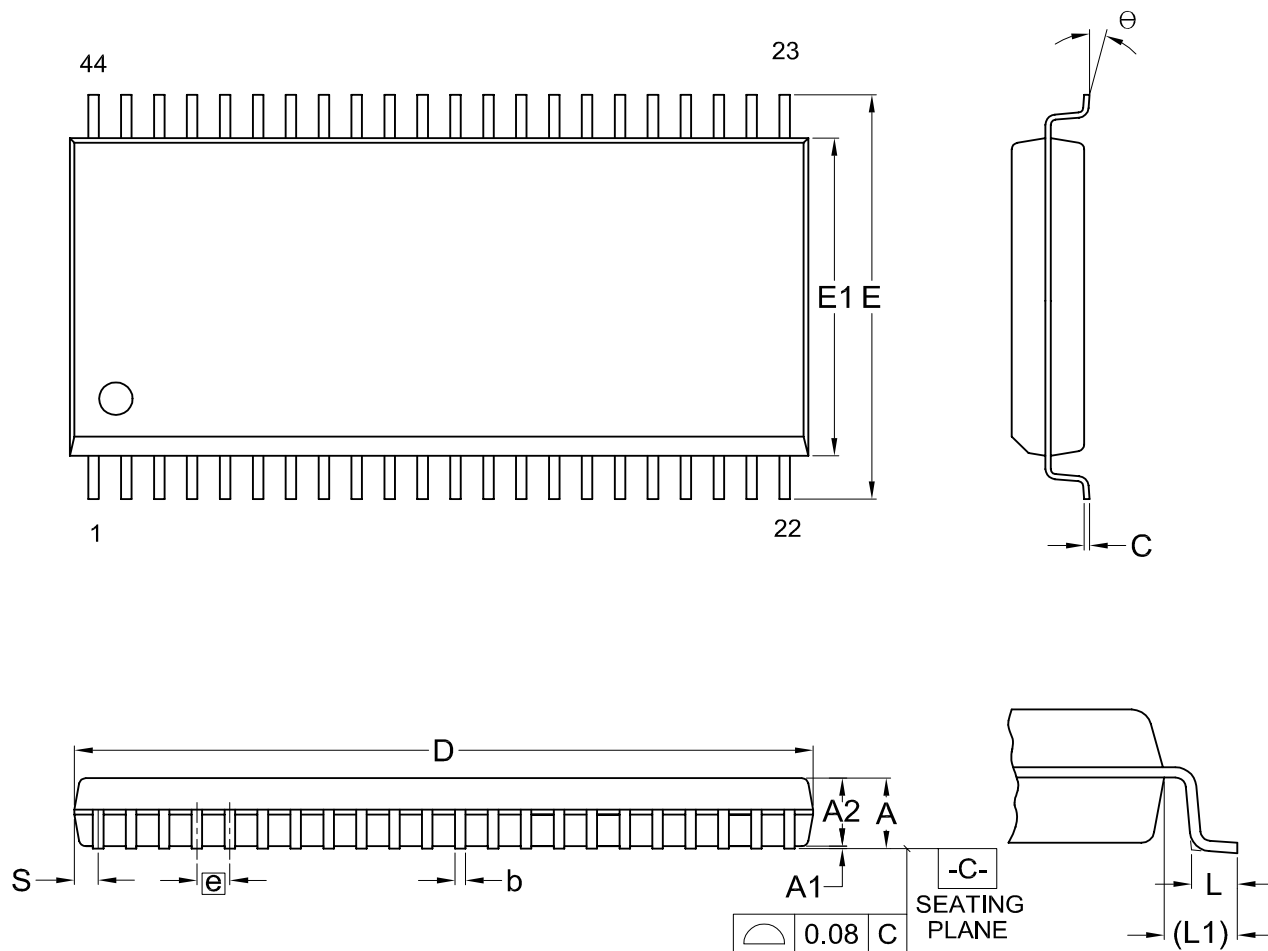


PAGE READ



PACKAGE INFORMATION

Title: Package Outline for SOP 44L (500MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
UNIT														
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	6	MO-175			11-26-'03



REVISION HISTORY

Revision	Description	Page	Date
0.01	1. Added Note 2 in AC Characteristics 2. Modified Input Pulse Levels from 0V~3.0V to 0.4V~2.4V	P2 P3	DEC/05/2005
0.02	1. Modified Operating Current from 20mA to 25mA 2. Added access time:100ns	P1,2 P1,2	JAN/10/2006
0.03	1. Removed access time:90ns 2. Modified random read timing	P1,2 P3	FEB/15/2006
0.04	1. Modified random read timing 2. Removed tAH in AC characteristics	P3 P2	APR/07/2006



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